IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:		Atty. Docket No.:	001701.00140
Ken Takeuchi et al.			
Serial No.:	10/073,999	Group Art Unit:	2827
Filed:	February 14, 2002	Examiner:	H. Ho
For:	Nonvolatile Semiconductor Memory Having Plural Data Storage Portions for a Bit Line Connected to Memory Cells	Confirmation No.:	9741

Pre-Appeal Brief Request For Review

U.S. Patent and Trademark Office
Customer Service Window, Mail Stop AF
Randolph Building
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Alexandria, VA 22314

Sir:

Applicants respectfully request review of the final rejection of March 14, 2006, in the above-identified application. No amendments are being filed with this request. This request is being filed with a Notice of Appeal. The review is requested for the reasons stated in the below remarks. If any fees are required or if an overpayment is made, the Commissioner is authorized to debit or credit our Deposit Account No. 19-0733, accordingly.

REMARKS/ARGUMENTS

Having received and reviewed the final Office Action dated March 14, 2006, and the Advisory Action dated May 31, 2006, Appellants respectfully submit that the current rejections are based on one or more clear errors, and that the appeal process can be avoided through a pre-appeal brief review as set forth in the Official Gazette notice of July 12, 2005. Claims 47-60, 63, 65, 66, and 92 are pending in this application. Support for the claims may be found at least in Figures 60A-60D of the present application.

The May 31, 2006, Advisory Action

The May 31, 2006, advisory action indicated that the claim amendments of May 14, 2006, would be entered but the rejections were not overcome. Applicants believe the rejections are in

error. Applicants address the rejections under 35 U.S.C. 112 and 35 U.S.C. 102.

Rejection of the Claims Under 35 U.S.C. 112

Claims 47, 48, 50, 55, and 56 stand rejected under 35 U.S.C. 112, second paragraph. Applicants modified the recitation addressed by the Examiner to separate the "common latch circuit" from the "common node". Applicants have addressed this issue but the Examiner did not indicate that this rejection had been overcome.

Claim 57 stands rejected under 35 U.S.C. 112, second paragraph.

Claim 57 has been further rejected as follows:

> "Claim 57, line 8, 'a third bit line connected to said second string line' is unclear and confusing. How does the 'second string [sic, bit] line' in line 5 of claim 57 relate to the 'second string [sic, ?] line' in line 7 of claim 57? Should 'third' be changed to –second—for clarifying?..."

Applicants traverse the Examiner's rejection of claim 57. The claim is not unclear. Claim 57 recites the following:

" 57. (Currently Amended) A nonvolatile semiconductor memory comprising:

a first string line including a first memory cell and a first select transistor connected in series;

a first bit line connected to said first string line;

a second bit line;

a second string line including a second memory cell and a second select transistor connected in series;

a third bit line connected to said second string line;

a fourth bit line;

..."

In other words, the claim recites, *inter alia*:

1) A first bit line
2) A second bit line
3) A third bit line

4) A fourth bit line

5) A first string line (connected to the first bit line)

6) A second string line (connected to the third bit line)

The relationship between these elements is clear from the claim. Applicants cannot modify the claim as suggested by the Examiner as the modification would make the claim confusing. Applicants believe the continued rejection of the claims under 112 is in error as the claims are not confusing or indefinite as the Examiner asserts.

Rejection of the Claims Over Hemink et al.

Claims 47-60, 62, 63, and 65-66 stand rejected under 35 U.S.C. § 102(a) over Hemink. Applicants traverse.

" 47. A nonvolatile semiconductor memory comprising:

a first string line including a first memory cell and a first select transistor connected in series;

a second string line including a second memory cell and a second select transistor connected in series;

a first bit line connected to said first string line;

a second bit line connected to said second string line, being different from said first bit line;

a common node connected to one ends of said first and second bit lines; and

a common latch circuit connected to said common node,

wherein first program /read data of said first memory cell is latched in said common latch circuit, while second program /read data of said second memory cell is held by said second bit line."

The claim recites 6 elements: a first string line, a second string line, a first bit line, a second bit line, a common node, and a common latch. In contrast, Hemink fails to show four separate lines (first string, second string, first bit, and second bit). According to Hemink, the first and second signal lines are in fact the same line. They are electrically shorted together. Because they are shorted together, they cannot be the first and second bit lines, respectively. The Examiner has listed one element of Hemink and asserted that it relates to two elements in

Applicants' claims. This is incorrect. See Figure 13 of Hemink. Hemink does not disclose the latch connected to two bit lines. With this structure, Hemink cannot realize the action that data of a first memory cell is latched in a latch circuit while data of a second memory cell is held by the second signal line as claimed.

Hemink does not disclose the operation of the first and second bit lines as claimed. The structure of Figure 13 does not disclose "first program /read data of said first memory cell is latched in said common latch circuit, while second program /read data of said second memory cell is held by said second bit line."

Hemink shows only first and second bit lines. While Hemink uses the term third and fourth bit lines (and the examiner equates these additional lines to the string lines and common node), these bit lines are in fact the same bit lines as the first and second bit lines respectively. This is in contrast to the claims above that distinguish the bit lines and distinctly claim the common node.

Accordingly, as Hemink fails to disclose each and every element of claim 47, the claim is allowable over Hemink.

Claims 48, 50, 55, 56, are allowable in that they recite similar recitations.

Dependent claims 49, 51-54, 58-60, 63, and 65-66 are allowable as they depend on allowable independent claims.

Rejection of the Claims Over Sakui

Claims 47-60, 62, 63, and 65-66 stand rejected under 35 U.S.C. § 102(e) over Sakui. Applicants traverse.

Claim 47 has been set forth above. The Examiner applies Figure 38 of Sakui to reject the claims. However, Figure 38 of Sakui does not relate to the recitations of claim 47. Column 33, lines 27-39 of Sakui indicates that the data circuit of Figure 38 relates to storing data in pairs.

> " FIG. 38 shows an arrangement using a differential sense amplifier. In this case, 1-bit data may be stored in two memory cell units as complementary data. Data is read by detecting a small difference between signal amounts (potentials) output from the two memory cell units and amplifying this difference. This allows a high-speed read.
>
> One-bit data is stored in a pair of memory cell units. For this reason, even when the program/erase endurance characteristics of one memory cell unit degrade due to the repeated data change operation, the reliability does not decrease as far as the other memory cell unit has satisfactory program/erase endurance characteristics."

Both the left and right side memory cells are accessed in parallel using BLi and /BLi. In other words, they operate the same way at the same time. This is different from the recitations of

claim 47.

In FIG. 38 of Sakui, a first bit line BLi is connected to a node of a latch circuit, which is different from a node of the latch circuit, a second bit line /BLi is connected to. In other words, as in FIGS. 13 and 20 of Hemnik, the first and second bit lines are not connected to a common node of the latch circuit. In addition, Sakui does not disclose that data of a first memory cell is latched in the latch circuit while data of a second memory cell is held in the second bit line. Therefore, the present invention is not anticipated by Sakui.

As Sakui fails to disclose each and every feature of claim 47, the claim is allowable over Sakui. Claims 48, 50, 55, 56 and 57 have been similarly amended and are believed allowable. Dependent claims 49, 51-54, 58-60, 63, and 65-66 are believed allowable as they depend on allowable independent claims.

For the above reasons, the rejections of the pending claims in the Final Office Action fail to establish *prima facie* obviousness. A pre-appeal finding that these claims are allowable is respectfully requested.

All issues having been addressed, Applicants respectfully submit that the instant application is in condition for allowance, and respectfully solicit prompt notification of the same. However, if for any reason the review panel believes the application is not in condition for allowance or there are any questions, the review panel is invited to contact the undersigned at (202) 824-3000.

Respectfully submitted,
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